A Fully Integrated PLL Frequency Synthesizer LSI for Mobile Communication System

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***Abstract* — A fully integrated phase locked loop (PLL) frequency synthesizer LSI has been developed. This newly developed fractional-N type PLL LSI consists of an on-chip loop filter and a voltage controlled oscillator (VCO) with an on-chip resonator circuit. This VCO has a band-switching tuning circuit using MOS capacitors and an analog tuning circuit using PN varactor diodes. Both these tuning circuits are controlled automatically without external adjustment. The phase noise of the VCO at 2.2 GHz is –92.5 dBc/Hz at 50 kHz offset, while the frequency switching time is 170us.**

I. Introduction

PLL circuits are used in various wireless application systems as a frequency synthesizer. Requirements for the PLL circuits are frequency switching time and phase noise. Unfortunately, these two characteristics have an inverse relationship, and they are optimized by characteristics of the loop filter design. However, there are some additional design issues when the VCO (including resonator circuits) is fully integrated on-chip. Some VCO designs have been reported in recent years [1], [2]. The VCO free run frequency varies widely, because of process variations related to the resonant tank inductor value, varactor diode, and the MIM capacitor as well as the characteristics of the oscillator transistor. Therefore, the VCO circuit is a key design element for any PLL system. In this paper, we describe a new VCO and PLL system that automatically changes the oscillation frequency band of the VCO by changing the capacitance of resonator circuit. This PLL operates over a wide frequency range for use in a frequency synthesizer system.

II. Process Technology

This LSI is fabricated with a 0.35 um BiCMOS process technology. The cut-off frequency (*fT)* of the NPN transistor is 20 GHz. The spiral inductor used in the resonant tank circuit is made of copper metalization, in order to achieve a high quality factor. The resonant tank circuit uses two types of capacitances to generate a wide tuning range. One capacitance type is a MOS capacitor, which has a 2.4 times variation ratio, while the other capacitance type is a PN varactor diode, with a 1.6 times variation ratio. In addition, metal inductors and MIM capacitors are also available for use in the IC design.

III. Circuit Design

One of the most important characteristics of a PLL circuit is the frequency switching time. Newly developed PLL logic in this device enables us to achieve fast frequency switching times by dedicated control circuit.

A. PLL Frequency Synthesizer

Fig. 1 shows the schematic diagram of the fractional-N PLL frequency synthesizer. The PLL frequency synthesizer consists of a *programmable divider*, a *phase comparator*, a *charge pump*, a *loop filter*, a *delta-sigma converter*, and a VCO. A significant difference in this synthesizer, as compared to conventional circuits is the frequency band-switching function and the *frequency error detector* in the synthesizer logic.

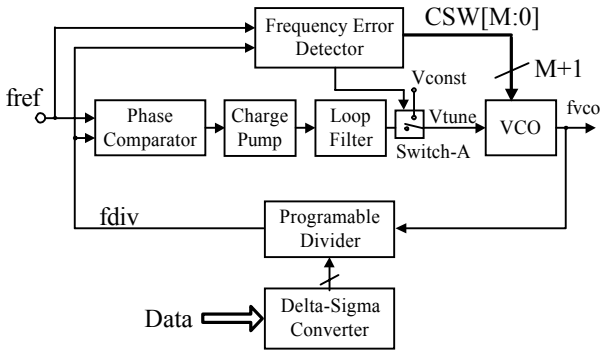

Fig. 1 PLL Frequency Synthesizer

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The VCO has frequency band-switching function in the resonator circuit. Depending on the required output frequency, the necessary VCO frequency band is selected by the control signals *CSW[M:0]*.

Fig. 2 shows the VCO resonant tank band-switching algorithm that automatically takes place each time when a new frequency data is set into the PLL. The resonant tank circuit has N frequency bands of operation, as shown by the different frequency versus tuning curves in Fig. 2.

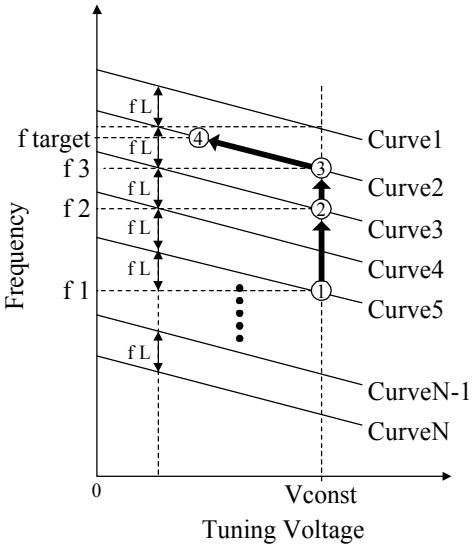

Fig. 2. VCO Frequency Bands

Once a new frequency data is set to the PLL, the *switch-A* is set to the constant voltage node, *Vconst*. The frequency band is selected to *Curve5* as shown in fig. 2 by the *CSW* signals. At this operation, the PLL loop is open loop condition and the VCO oscillates at the frequency of *f1*. The *frequency error detector* estimates the final target frequency by comparing the frequency difference between *fdiv* and *fref*, and referring the conversion table, and then generates *CSW* signals to select the new curve. The *fdiv* is the output signal of *programmable divider* and the *fref* is the reference clock. In Fig. 2, the final target frequency is not on the *Curve5*, then the frequency band is changed to *Curve3* and the VCO oscillates at the frequency of *f2*. The frequency difference between the target and *f2* is more than *fL*, therefore the band is changed to *Curve2*. However, the target frequency might not be on this selected band because of mismatch between *fL* and table data caused by process variations in mass production in actual LSI. In case of missing band, the *frequency error detector* iterates this operation over until the frequency difference between the VCO and the target become less than *fL*. Once frequency band is fixed, the *switch-A* is set to the *loop filter* output, and the PLL loop becomes closed loop condition. The *phase comparator* compares the *fdiv* with the *fref* as a regular PLL frequency synthesizer.

B. VCO

Fig. 3 shows the schematic diagram of the VCO along with a detailed schematic of the parallel *LC* resonant tank. The VCO circuit is differential topology, which use the cross-coupling of capacitors *C1* and *C2* to generate positive feedback and therefore create the negative resistance condition required for oscillation to occur. The parallel *LC* resonant tank present at the collector of transistors *Q1* and *Q2* determines the oscillation frequency of the VCO. Transistor *Q3,* combined with resistor *R3* and capacitor *C5,* serve as a ripple filter to help suppress the noise from the power supply input *Vcc*. The equivalent capacitance *Ct* of the parallel LC tank circuit actually consists of two PN Varactors (*P1*, and *P2*), two MIM capacitors (*C3*, and *C4*), and MOS capacitors (*M1* through *Mn*). Assuming that the capacitance of varactor *P1* is *Cv*, capacitor *C3* is *C*, the capacitance of the MOS capacitors *M1*, *M3*, *M5*, and *Mn-1* are *Cm1*, *Cm2*, *Cm3*, and *CmM+1*, and inductor *L0* is *L0*, then the oscillation frequency of the VCO can be calculated using equation (1).

$$fosc = \frac{1}{2\pi}\sqrt{\frac{L0}{2}\left(\frac{C\times Cv}{C+Cv} + Cm1 + Cm2 + Cm3\cdots + CmM + 1\right)} \quad (1)$$

The VCO's tuning voltage range is determined by the series combination of the capacitance variation ratio of this PN varactor and the ac-coupling capacitors. The PN varactor diode is actually formed from an array of several separate varactors, in order to minimize the series resistances of the complete PN varactor diode. The capacitance versus tuning voltage characteristic for the complete PN varactor diode is shown in Fig. 4. The complete PN varactor is designed to maximize the capacitance variation ratio over the desired analog tuning voltage range.

The MOS capacitors are used in the two "flat" regions of their capacitance curve, as shown in Fig. 5. In order to maintain low phase noise operation of the VCO, the control voltages (from control signals *CSW[M:0]*) are determined to minimize the series resistance of the MOS capacitors. The band-switching range and step size are determined by the capacitance variation ratio of these MOS capacitors.

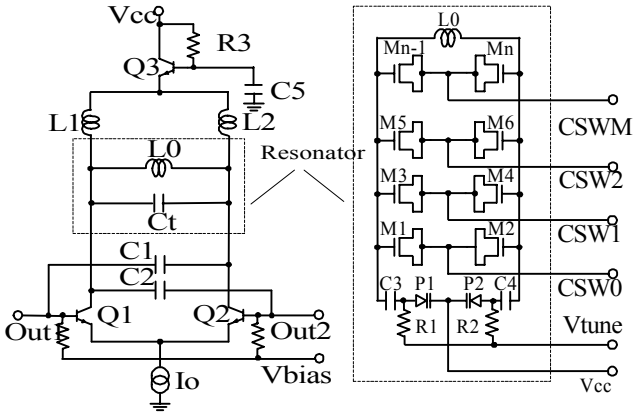

Fig. 3 VCO & LC parallel resonator schematics

The inductor used in the VCO resonant tank circuit is formed by the use of on-chip copper metal, in order to get a high quality factor at the desired operating frequencies.

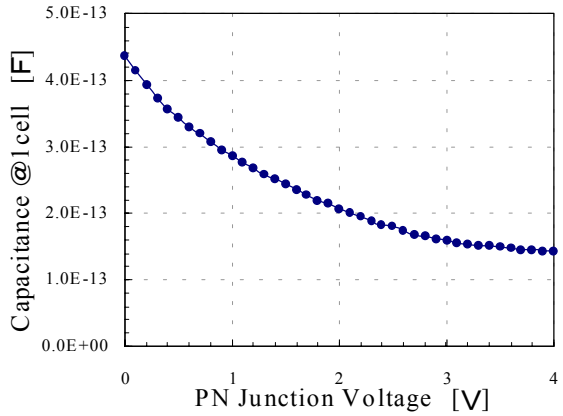

Fig. 4 PN Varactor Diode Capacitance vs. Tuning Voltage

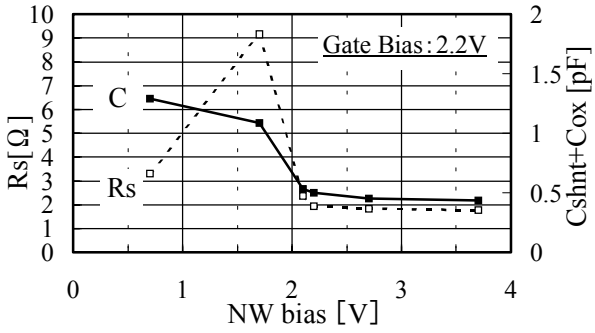

Fig. 5 MOS Capacitor capacitance and Series Resistance (Measured)

Fig. 6 shows the schematic diagram of the VCO Buffer Amplifier, which is formed by the cascade connection of a differential pair of NPN transistors.

Fig. 7 shows the frequency range versus tuning voltage characteristic of the VCO for the typical bands of operation. A tuning range of 490 MHz - from 1.85 to 2.34 GHz - is achieved with a tuning voltage range from 0.0 to 3.0 V.

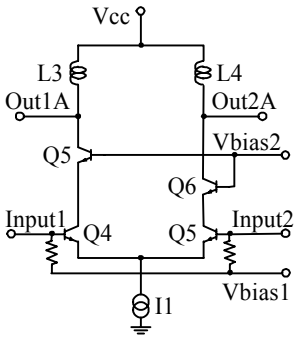

Fig. 6 VCO Buffer Amplifier

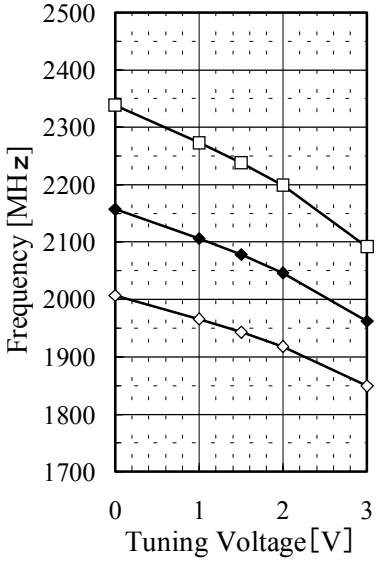

Fig. 7 VCO Frequency Range vs. Tuning Voltage

IV. Performance

This PLL LSI is packaged in a leadless plastic package. The measurements shown were taken with an output connected to the VCO/PLL signal analyzer. The spectrum of the VCO is shown in Fig. 8. At an oscillation frequency of 2.2 GHz, phase noise of -92.5 dBc/Hz at 50 KHz offset and –119.8 dBc/Hz at 1 MHz offset was achieved.

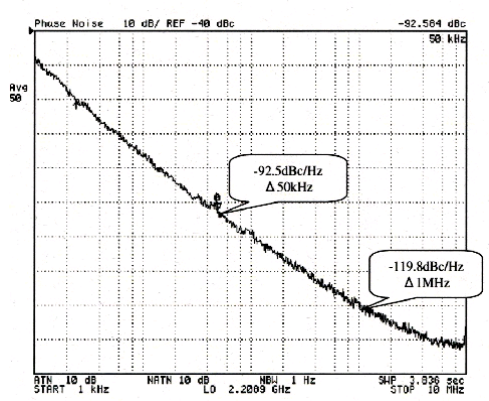

Fig. 8 VCO Phase Noise

Fig. 9 shows the frequency switching time. This time is defined as oscillator frequency settling time within 300 Hz of the desired frequency. The PLL synthesizer control data was configured to change the oscillation frequency from 2200 MHz to 2260 MHz. In this measurement, band-switching operation is done once and then the PLL is set to the closed loop. The frequency switching time was 170 us. The performance of the developed PLL frequency synthesizer LSI is summarized in Table 1. Fig. 10 shows a photograph of this LSI.

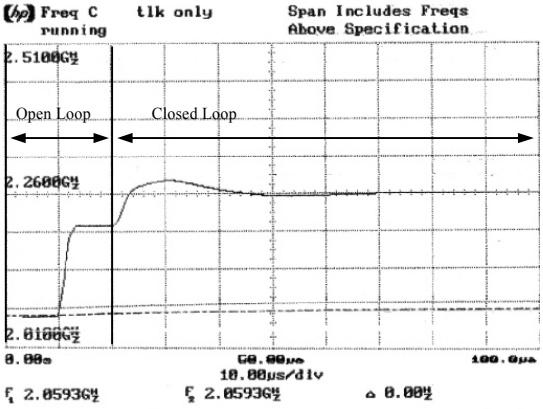

Fig. 9 PLL Frequency Switching Time

TABLE 1
Summary of PLL Frequency Synthesizer Performance

Parameter	Value
Supply Voltage	3.0 V
Total Current	17 mA
Lock frequency range	1910 to 2340 MHz
Phase Noise @ 50kHz Offset	-92.5 dBc/Hz
Phase Noise @ 1MHz Offset	-119.8 dBc/Hz
Frequency Switching Time, to within 300 Hz	170 us

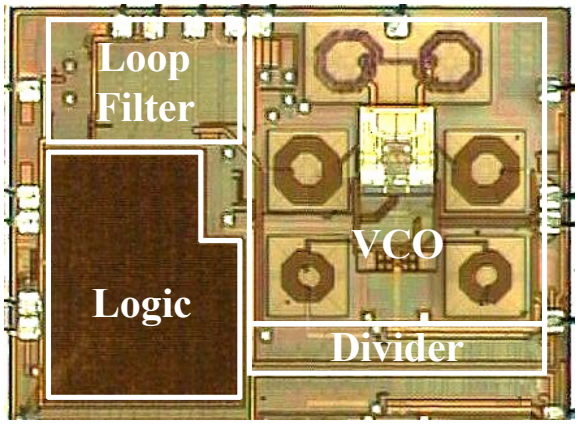

Fig. 10 Microphotograph of fabricated LSI

V. Conclusion

A new fully-integrated PLL frequency synthesizer LSI has been developed. This PLL LSI consists of a fully-integrated monolithic VCO, including an internal resonator circuit. The VCO has a wide frequency oscillation range of 490 MHz. The PLL using this VCO has an acquisition frequency range of 430 MHz. This range is enough to cover the large shifts in the oscillation frequency caused by process variations and/or temperature variations. Phase noise of -92.5 dBc/Hz at 50 kHz offset at a 2.2 GHz oscillation frequency was obtained, and also a fast frequency switching time of 170 us is achieved. This PLL LSI is suitable for cellular phone, to help minimize the number of external components.

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References

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[2] A. Kral, F. Behbahani, and A. A. Abidi "RF-CMOS Oscillators with Switched Tuning" *Custom IC Conference*, pp.555-558, May 1998.